This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Currently Amended) A method of filtering an external cache snoop probe to a first cache, the method comprising:

determining a cache line state, the cache line state being associated with the external cache snoop probe and a cache line in a second cache; and

posting a hit-modified signal if the cache line state is an enhanced exclusive state, wherein the enhanced exclusive state indicates a copy of the cache line is in the first cache in a modified state and that the cache line in the second cache is unmodified.

2. (Original) A method as defined in claim 1, further comprising posting the hit-modified signal if the cache line state is an enhanced modified state, wherein the enhanced modified state indicates a copy of the cache line may be in the first cache.

3. (Original) A method as defined in claim 2, further comprising posting the hit-modified signal if the cache line state is a modified state, wherein the modified state indicates the second cache owns the cache line and the first cache does not own the cache line.

4. (Original) A method as defined in claim 1, further comprising sending a snoop-to-invalidate probe to the first cache after posting the hit-modified signal.

5. (Original) A method as defined in claim 1, wherein the external cache snoop probe is sent to the second cache, a second cache write-back queue, and an intermediate

structure between the first cache and the second cache.

6. (Original) A method as defined in claim 1, wherein the external cache snoop probe is sent only to the second cache, a second cache write-back queue, and an intermediate structure between the first cache and the second cache.

7. (Original) A method as defined in claim 1, further comprising determining a snoop type associated with the external cache snoop probe is one of a snoop-to-share type and a snoop-to-invalidate type.

8. (Currently Amended) An apparatus to filter a cache snoop probe, the apparatus comprising:

a first cache;

a second cache;

a memory controller operatively coupled to the first cache and the second cache, the memory controller being structured to (i) determine a cache line state associated with a cache line in the second cache, the cache line in the second cache being identified by the cache snoop probe, and (ii) post a hit-modified signal if the cache line state is an enhanced exclusive state, wherein the enhanced exclusive state indicates a copy of the cache line is in the first cache in a modified state and that the cache line in the second cache is unmodified.

9. (Original) An apparatus as defined in claim 8, wherein the memory controller is structured to post the hit-modified signal if the cache line state is an enhanced modified state, wherein the enhanced modified state indicates a copy of the cache line may be in the

first cache.

10. (Original) An apparatus as defined in claim 8, wherein the memory controller is structured to post the hit-modified signal if the cache line state is a modified state, wherein the modified state indicates the second cache owns the cache line and the first cache does not own the cache line.

11. (Original) An apparatus as defined in claim 8, wherein the memory controller is structured to send a snoop-to-invalidate probe to the first cache after posting the hit-modified signal.

12. (Original) An apparatus as defined in claim 8, further comprising:

a main memory;

a write-back queue operatively coupled to the second cache and the main memory; and

an intermediate structure operatively coupled to the first cache and the second cache, wherein the cache snoop probe is sent to the second cache, the write-back queue, and the intermediate structure.

13. (Original) An apparatus as defined in claim 8, further comprising:

a main memory;

a write-back queue operatively coupled to the second cache and the main memory; and

an intermediate structure operatively coupled to the first cache and the second cache, wherein the cache snoop probe is sent only to the second cache, the write-back queue,

and the intermediate structure.

14. (Original) A method of filtering an external cache snoop probe to a first cache, the method comprising:

determining a snoop type associated with the external cache snoop probe;

determining a cache line state, the cache line state being associated with the external cache snoop probe and a cache line in a second cache;

posting a hit signal if (i) the snoop type is a snoop-to-share type, (ii) the cache line state is a shared state, and (iii) the second cache posts a write-back miss signal; and

sending a snoop-to-share probe to the first cache after posting the hit signal if the hit signal is posted.

15. (Original) A method as defined in claim 14, further comprising posting a no hit signal if (i) the snoop type is the snoop-to-share type, (ii) the cache line state is the shared state, and (iii) the second cache posts a write-back hit signal.

16. (Original) A method as defined in claim 15, further comprising posting a no hit modified signal if (i) the snoop type is the snoop-to-share type, (ii) the cache line state is the shared state, and (iii) the second cache posts the write-back hit signal.

17. (Original) A method as defined in claim 16, further comprising sending a snoop-to-invalidate probe to the first cache after posting the no hit signal and the no hit modified signal.

18. (Original) An apparatus to filter a cache snoop probe, the apparatus comprising:

a first cache;

a second cache;

a memory controller operatively coupled to the first cache and the second cache, the memory controller being structured to (i) determine a snoop type associated with the cache snoop probe, (ii) determine a cache line state associated with a cache line in the second cache, the cache line in the second cache being identified by the cache snoop probe, and (iii) post a hit signal if (a) the snoop type is a snoop-to-share type, (b) the cache line state is a shared state, and (c) the second cache posts a write-back miss signal.

19. (Original) An apparatus as defined in claim 18, wherein the memory controller is structured to post a no hit signal if (d) the snoop type is the snoop-to-share type, (e) the cache line state is the shared state, and (f) the second cache posts a write-back hit signal.

20. (Original) An apparatus as defined in claim 19, wherein the memory controller is structured to post a no hit modified signal if (d) the snoop type is the snoop-to-share type, (e) the cache line state is the shared state, and (f) the second cache posts the write-back hit signal.

21. (Original) A method of filtering an external cache snoop probe to a first cache, the method comprising:

determining a snoop type associated with the external cache snoop probe;

determining a cache line state, the cache line state being associated with the

external cache snoop probe and a cache line in a second cache; and

sending a snoop-to-share probe to the first cache if (i) the snoop type is a snoop-to-share type, (ii) the cache line state is an exclusive state, and (iii) the second cache posts a write-back miss signal.

22. (Original) A method as defined in claim 21, further comprising:

receiving a response to the snoop-to-share probe from the first cache; and

posting one of a hit signal and a hit modified signal based on the response to the snoop-to-share probe.

23. (Original) A method as defined in claim 22, further comprising sending a snoop-to-invalidate probe to the first cache if (i) the snoop type is the snoop-to-share type, (ii) the cache line state is the exclusive state, and (iii) the second cache posts a write-back hit signal.

24. (Original) A method as defined in claim 23, further comprising:

receiving a response to the snoop-to-invalidate probe from the first cache; and

posting one of the hit signal and the hit modified signal based on the response to the snoop-to-invalidate probe.

25. (Original) An apparatus to filter a cache snoop probe, the apparatus comprising:

a first cache;

a second cache;

a memory controller operatively coupled to the first cache and the second

cache, the memory controller being structured to (i) determine a snoop type associated with the cache snoop probe, (ii) determine a cache line state associated with a cache line in the second cache, the cache line in the second cache being identified by the cache snoop probe, and (iii) send a snoop-to-share probe to the first cache if (a) the snoop type is a snoop-to-share type, (b) the cache line state is an exclusive state, and (c) the second cache posts a write-back miss signal.

26. (Original) An apparatus as defined in claim 25, wherein the memory controller is structured to:

receive a response to the snoop-to-share probe from the first cache; and

post one of a hit signal and a hit modified signal based on the response.

27. (Original) An apparatus as defined in claim 25, wherein the memory controller is structured to send a snoop-to-invalidate probe to the first cache if (d) the snoop type is the snoop-to-share type, (e) the cache line state is the exclusive state, and (f) the second cache posts a write-back hit signal.

28. (Original) An apparatus as defined in claim 27, wherein the memory controller is structured to:

receive a response to the snoop-to-invalidate probe from the first cache; and

post one of a hit signal and a hit modified signal based on the response.

29. (Original) A method of filtering an external cache snoop probe to a first cache, the method comprising:

determining a snoop type associated with the external cache snoop probe;

determining a cache line state, the cache line state being associated with the external cache snoop probe and a cache line in a second cache;

posting a no hit signal and a no hit modified signal if (i) the snoop type is a snoop-to-invalidate type, and (ii) the cache line state is a shared state; and

sending a snoop-to-invalidate probe to the first cache after posting the no hit signal and the no hit modified signal.

30. (Original) A method as defined in claim 29, further comprising sending the snoop-to-invalidate probe to the first cache if (i) the snoop type is the snoop-to-invalidate type, and (ii) the cache line state is an exclusive state.

31. (Original) A method as defined in claim 30, further comprising posting one of the hit modified signal and the no hit modified signal based on a response to the snoop-to-invalidate probe.

32. (Original) A method as defined in claim 29, further comprising posting the no hit signal and the no hit modified signal if (i) the snoop type is the snoop-to-invalidate type, and (ii) the cache line state is an exclusive state.

33. (Original) An apparatus to filter a cache snoop probe, the apparatus comprising:

a first cache;

a second cache;

a memory controller operatively coupled to the first cache and the second cache, the memory controller being structured to (i) determine a snoop type associated with

the cache snoop probe, (ii) determine a cache line state associated with a cache line in the second cache, the cache line in the second cache being identified by the cache snoop probe, and (iii) post a no hit signal and a no hit modified signal if (a) the snoop type is a snoop-to-invalidate type, and (b) the cache line state is a shared state.

34. (Original) An apparatus as defined in claim 33, wherein the memory controller is structured to send a snoop-to-invalidate probe to the first cache after posting the no hit signal and the no hit modified signal.

35. (Original) An apparatus as defined in claim 33, wherein the memory controller is structured to send a snoop-to-invalidate probe to the first cache if (c) the snoop type is the snoop-to-invalidate type, and (d) the cache line state is an exclusive state.

36. (Original) An apparatus as defined in claim 35, wherein the memory controller is structured to post one of a hit modified signal and no hit modified signal based on a response to the snoop-to-invalidate probe.

37. (Original) An apparatus as defined in claim 35, wherein the memory controller is structured to post the no hit signal and the no hit modified signal if (i) the snoop type is the snoop-to-invalidate type, and (ii) the cache line state is the exclusive state.

38. (Original) A method of filtering an external cache snoop probe to a first cache, the method comprising:

determining a snoop type associated with the external cache snoop probe;

determining a cache line state, the cache line state being associated with the

external cache snoop probe and a cache line in a second cache;

posting a hit signal if (i) the snoop type is a snoop-to-share type, (ii) the cache line state is an exclusive state, and (iii) the second cache posts a write-back miss signal; and

sending a snoop-to-share probe to the first cache if (i) the snoop type is a snoop-to-share type, (ii) the cache line state is an exclusive state, and (iii) the second cache posts a write-back miss signal.

39. (Original) A method as defined in claim 38, further comprising posting a no hit signal and a no hit modified signal if (i) the snoop type is the snoop-to-share type, (ii) the cache line state is the exclusive state, and (iii) the second cache posts a write-back hit signal.

40. (Original) A method as defined in claim 39, further comprising sending a snoop-to-invalidate probe to the first cache after posting the no hit signal and the no hit modified signal if (i) the snoop type is the snoop-to-share type, (ii) the cache line state is the exclusive state, and (iii) the second cache posts the write-back hit signal.

41. (Original) An apparatus to filter a cache snoop probe, the apparatus comprising:

a first cache;

a second cache;

a memory controller operatively coupled to the first cache and the second cache, the memory controller being structured to (i) determine a snoop type associated with the cache snoop probe, (ii) determine a cache line state associated with a cache line in the second cache, the cache line in the second cache being identified by the cache snoop probe, and (iii) post a hit signal if (a) the snoop type is a snoop-to-share type, (b) the cache line state

is an exclusive state, and (c) the second cache posts a write-back miss signal.

42. (Original) An apparatus as defined in claim 41, wherein the memory controller is structured to send a snoop-to-share probe to the first cache if (d) the snoop type is the snoop-to-share type, (e) the cache line state is the exclusive state, and (f) the second cache posts the write-back miss signal.

43. (Original) An apparatus as defined in claim 41, wherein the memory controller is structured to post a no hit signal and a no hit modified signal if (d) the snoop type is the snoop-to-share type, (e) the cache line state is the exclusive state, and (f) the second cache posts a write-back hit signal.

44. (Original) An apparatus as defined in claim 43, wherein the memory controller is structured to send a snoop-to-invalidate probe to the first cache after posting the no hit signal and the no hit modified signal if (g) the snoop type is the snoop-to-share type, (h) the cache line state is the exclusive state, and (j) the second cache posts the write-back hit signal.